Safety Integrity Level (SIL) Determination and Verification Training Course

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Rome (Italy)



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Introduction:

Safety Integrity Level SIL determination and verification is the systematic engineering process of quantifying risk reduction requirements for hazardous industrial processes and mathematically validating that safety instrumented functions achieve those required statistical targets. This one-week course equips instrumentation, control, and process safety professionals to construct a complete SIL Determination and Verification Dossier. Taught at practitioner depth through a hands-on modelling build practical mode, the course examines the international standard IEC 61511-1:2016 from the International Electrotechnical Commission alongside parent standard IEC 61508:2010. Engineers master Safety Integrity Level SIL determination and verification with Blackbird Training Centre to ensure defensible operational asset integrity.

Course Objectives:

- Distinguish between target risk reduction during SIL determination and achieved risk reduction during hardware SIL verification.
- Compare semi-quantitative Layer of Protection Analysis credits against qualitative calibrated Risk Graph matrices for assigning target safety integrity levels.
- Select appropriate Hardware Fault Tolerance architectures and redundant voting configurations to satisfy normative architectural constraints.
- Apply mathematical failure rate equations to calculate Probability of Failure on Demand and Mean Time to Fail Spurious.
- Interpret Clause 10 Safety Requirements Specification parameters to translate process hazard findings into functional design specifications.
- Justify proof-test intervals, diagnostic test coverage, and common cause failure assumptions across safety instrumented systems.

Target Audience:

- Process safety engineers responsible for facility risk assessments who must decide whether documented independent protection layers justify required risk reductions.
- Instrumentation and control engineers responsible for emergency shutdown loop design who must select compliant logic solvers, sensors, and final elements.
- Reliability and asset integrity engineers responsible for plant maintenance strategies who must determine adequate proof-test procedures and testing intervals.
- Operations risk and compliance specialists responsible for safety lifecycle governance who must evaluate whether functional safety assessments satisfy international standards.



Course Outline:

Day 1: Functional Safety Fundamentals and Risk Assessment Foundations

- HAZOP Findings vs LOPA Mitigations: Establishing Process Hazard Boundaries and Initial Initiating Event Frequencies
- IEC 61511-1:2016 Framework: Navigating the Safety Instrumented System Lifecycle Phases for Industrial Process Environments
- Tolerable Risk Targets: Establishing Corporate Calibrated Consequence Matrices and Environmental Fatality Risk Thresholds
- Safety Instrumented Function Definition: Identifying Specific Process Trip Actions, Protective Parameters, and Safe States
- Independent Protection Layer Criteria: Verifying Independence, Dependability, and Auditability Metrics for Active Layers

Day 2: Target SIL Determination Methods and Safety Requirements Specifications

- Calibrated Risk Graph vs LOPA Methodology: Comparing Allocation Rigour for Target Protection Layer Credits
- Layer of Protection Analysis Execution: Evaluating Initiating Event Frequencies, Enabling Conditions, and Protection Credits
- Safety Requirements Specification Development: Translating Process Interlock Demands into IEC 61511 Clause 10 Clauses
- SIS Security Risk Assessments: Integrating Cybersecurity Mitigations for Safety Logic Solvers and Networks
- Functional Safety Assessment Stage 1: Reviewing Hazard Identification and Allocation Rigour Prior to Engineering Design

Day 3: SIL Verification Mechanics and Architectural Constraints

- IEC 61508 vs IEC 61511 Architectural Rules: Comparing Route 1H and Route 2H Constraints
- Hardware Fault Tolerance Requirements: Selecting Sensor and Actuator Redundancy Based on Subsystem Failure Data
- Safe Failure Fraction Analysis: Calculating Undetected Safe and Dangerous Device Breakdown Fractions Across Subsystems
- Prior Use Justification: Documenting Operating Experience and Proven-in-Use Evidence for Uncertified Field Instrumentation
- Logic Solver Architectures: Evaluating Programmable Electronic Logic Controllers and Internal Redundant Processing Channels



Day 4: Quantitative Modelling of Failure Probabilities and Spurious Trips

- Low Demand PFDavg vs High Demand PFH: Selecting Mathematical Reliability Models for Industrial Trip Frequencies
- Common Cause Failure Analysis: Applying the Beta Factor Estimation Method to Multi-Channel Redundant Loops
- Spurious Trip Rate Calculations: Modeling Mean Time to Fail Spurious Across Differing Redundant Architectures
- Diagnostic Coverage Effects: Quantifying Automated Dangerous Detection Coverage and Online Loop Self-Testing Impacts
- Proof Testing Interval Impact: Calculating Probability of Failure on Demand Across Varied Mechanical Overhaul Schedules

Day 5: Modelling Build: Assembly of the Complete Determination and Verification Dossier

- Voting Architecture Comparison: Evaluating 1oo2 vs 2oo3 Voting Architectures for Reliability and Process Availability
- Loop Reliability Calculation: Synthesising Sensor, Logic Solver, and Final Element Data to Verify Compliance
- Proof-Test Procedure Design: Specifying Testing Steps, Diagnostic Bypass Controls, and Partial Stroke Valve Protocols
- Functional Safety Assessment Stage 2 and 3: Executing Stage Assessments Prior to Commissioning and Initial Operation
- Dossier Finalisation: Completing the Formal SIL Determination and Verification Dossier for Operational Deployment

Skills You Will Gain:

- Hazard Consequence Profiling
- LOPA Risk Allocation
- Safety Requirements Specification Drafting
- Hardware Fault Tolerance Evaluation
- PFDavg Reliability Calculations
- Spurious Trip Rate Modelling
- Beta-Factor Common Cause Assessment
- Functional Safety Audit Planning



Why Attend This Course:

- From relying on subjective intuition for instrumented protection targets to conducting systematic, auditable Layer of Protection Analysis calculations.
- From treating failure rates as static vendor values to computing precise Probability of Failure on Demand based on proof-test intervals and diagnostic coverage.
- From uncertain hardware redundancy choices to confidently selecting compliant architectures that balance functional safety with plant availability.
- From disconnected lifecycle documentation to building and assembling an auditable SIL Determination and Verification Dossier.

Conclusion:

Safety Integrity Level determination and verification provides the quantitative foundation for designing and maintaining trustworthy emergency shutdown systems in hazardous processing facilities. This course resolves key industry distinctions between qualitative risk ranking and semi-quantitative protection layer allocation, minimum architectural fault tolerance and computational probability of failure on demand, and safety reliability versus nuisance spurious trip avoidance. Tailored for operational engineers, instrumentation specialists, and risk analysts requiring rigorous practitioner depth, this course delivers the mathematical and procedural capability to validate safety-critical functions with confidence.

Frequently Asked Questions FAQ:

What is Safety Integrity Level determination and verification?

Safety Integrity Level determination and verification is the engineering discipline of assessing process risks to assign necessary target risk-reduction levels to safety instrumented functions and mathematically proving that the selected hardware, architectures, and testing frequencies satisfy those probabilistic performance targets.

What is the difference between SIL determination and SIL verification?

SIL determination identifies the risk-reduction target required to bring an unmitigated process hazard below a tolerable threshold, whereas SIL verification is the subsequent engineering calculation confirming that the chosen instruments, redundancy, failure rates, and proof-testing intervals meet or exceed that assigned target.

Which international standard governs Safety Integrity Level determination and verification?

Safety Integrity Level determination and verification for the process sector is governed by IEC 61511-1:2016, which defines the safety lifecycle and requirements for instrumented systems, supported by the umbrella generic functional safety standard IEC 61508:2010 for product design and component failure statistics.



Is Safety Integrity Level determination and verification suitable for an instrumentation engineer?

Yes, this course is designed for operational instrumentation engineers responsible for selecting hardware, configuring redundant voting channels, calculating probability of failure on demand, and drafting safety requirement specifications aligned with international safety lifecycles.

